Industrial Processes Automation

MSc in Electrical and Computer Engineering
Winter Semester 2016/2017
1st Exam, 19th January 2017

Read all questions of the exam carefully before starting to answer.
- *Provide detailed justifications to all answers.*
- *The use of bibliographic material, either in paper or in digital format is allowed.*
- *Exchange of information is forbidden (e.g. voice, WiFi, Bluetooth, GPRS, WAP,…).*
- *Exam duration: 3 hours.*

Q1. *Store one logic value:* (i) Write one ST program that saves the value of the input **%i0.2.0** to the output **%q0.4.0** when the input **%i0.2.1** is true. If **%i0.2.1** is false then the program keeps the previous output value. (ii) Solve the same problem using Ladder. (iii) Show that the problem can be solved with one logic function (hint: build a logic table computing %q0.4.0 from its previous value and the current inputs).

Q2. S*can cycle:* Consider that the ladder diagram in the next figure is the single code run by a PLC, in a MAST section configured to be cyclic. The PLC input and output take **2msec+2msec** and each ladder instruction (contact read, coil write, timer) takes about **1msec**. At **t=0** the outputs **%q0.2.1** and **%q0.2.2** have the logic value False. The timers have preset values of **2sec** and **8sec**. (i) Indicate the scan period of the PLC. (ii) Sketch the time responses of **%q0.2.1** and **%q0.2.2**. (iii) Estimate the time **%q0.2.1** is ON if the program runs one hour.
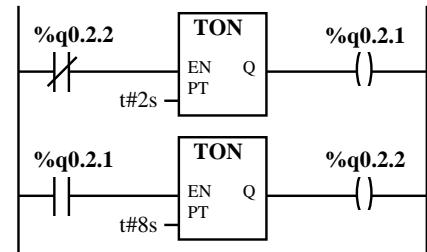

Q3. *ST program:* Consider the objective of turning ON the output **%q0.3.15** after a **5 minutes** delay triggered by a positive edge trigger in the input **%i0.3.0**. A negative edge trigger turns OFF the output. (i) Write one ST program based in one timer. (ii) Write an alternative program not using timers or counters. Assume that the scan cycle period is **10msec**. Use **%MW0** to count scan cycles. Use other auxiliary variables as needed. (iii) While using **%MW0** propose changes in case the time delay needs to be set to **10 minutes** or **1 day**.

Q4. *Turing Machine*. The next figure shows the Finite State Machine (FSM) of a *2-state Busy Beaver Turing Machine* and a short description on how the magnetic tape works. The notation *I/JK* on the arcs means input *I* and output *JK*. For example, **0/1L** means "if input **0** is read from the tape, then output (write) **1** to the same tape location, and finally move the tape **Left** one position".

a) Ignoring the outputs of the FSM, propose one Petri Net (PN) similar to the FSM. Indicate the incidence matrix and discuss the liveness properties of the transitions of the PN. Note that in this question the tape is not considered.

b) Make the reachability tree for the PN created in (a). Study the coverability, safeness, boundedness and conservation properties of the PN. Indicate a minimum sequence of transitions for the FSM to reach the Halt state and choose a non-empty tape that provides that sequence.
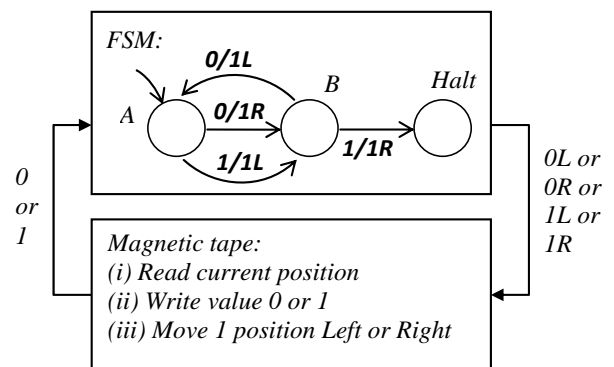
c) Comment the next sentence: "If outputs are associated to PN places, not transitions, then one needs the PN to have more places than the number of states of the FSM". Suggest a way to improve the PN model in order to contain outputs.

d) If one runs the PN (FSM) in conjunction with an initially empty tape, how many "ones" does the tape have after reaching the halting place? Does this information contradict the liveness determined in (a)?

Q5. *Supervision based modelling:* RS232 serial communication between computers, still available nowadays mainly through USB, is usually based on Universal Asynchronous Receiver/Transmitter (UART) chips. First UART chips encompassed two 8-bytes buffers in order to save time to the main CPU. UARTs transmit/receive one byte at a time, bit-by-bit. In this problem we model the number of bytes existing at each moment in the buffers.
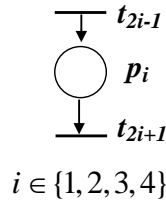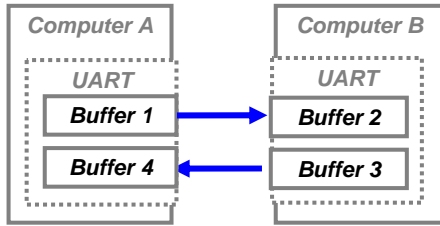
a) Consider one Petri net, as shown in the figure, for each one of the four buffers. The initial marking is zero for all places. Using the method of supervision based on marking invariants impose that the four buffers are limited to having at most 8 bytes. Note: In this question the buffers are considered separated, therefore detail computations just for Buffer 1 and build a complete incidence matrix by replicating the supervisor for the other buffers.

b) Using the method of marking invariants, considering generalized constraints, formulate the necessary supervisors to represent sending of bytes (i) from Buffer 1 to Buffer 2 and (ii) from Buffer 3 to Buffer 4. Enforce that at most one byte is being sent at each time. Hint: In many problems the general expressions for computing the supervisor can be simplified.

c) Using the method of matrix equations find one minimal operation cycle.

d) One may conjecture that the constraints associated to the sequence or quantity of firings can be rewritten with simple linear constraints by adding an arc and an auxiliary place at the output of the transitions under consideration. Propose constraints such that messages sent by Computer A through Buffer 1 and Buffer 2 are acknowledged by Computer B, byte by byte, through Buffer 3 and Buffer 4. The new constraints should keep conservation of the complete Petri net. Draw the complete Petri net including all the supervisors.

Q6. *Unobservable transitions.* Consider a Petri net $C = \left(P, T, D^+, D^-, \mu_0\right)$, $P = \{p_1, p_2, p_3\}$, $T = \{t_1, t_2, t_3\}$, D^+ and D^- denote pre and post incidence matrices, $D = D^+ - D^-$, $\mu_0 = \mu_p(0)$ is the initial state.

a) Prove that for any reachable state $\mu_p(k)$ one has $\mu_p(k) \in IN_0^3$ given the general definition of a Petri net and in particular $D^- q(k) \leq \mu_p(k)$. Notation: IN_0 is the set of natural numbers including zero.

b) Consider that one wants to impose a linear constraint $L\mu_p \leq b$, where t_3 is unobservable, in the case of the specific following data:

$$D = \begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & -1 \\ -1 & -1 & 2 \end{bmatrix}, \; \mu_0 = \begin{bmatrix} 1 \\ 1 \\ 0 \end{bmatrix}, \; L = \begin{bmatrix} 1 & 0 & 1 \\ 0 & 1 & 1 \end{bmatrix}, \; b = \begin{bmatrix} -1 \\ -1 \end{bmatrix}, \; R_1 = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 0 & 1 \end{bmatrix}, \; R_2 = \begin{bmatrix} 2 & 0 \\ 0 & 2 \end{bmatrix}.$$

Let $L_a = R_1 + R_2 L$ and $b_a = R_2(b+1) - 1$. Prove that the solutions $\mu_p \in IN_0^3$ of $L_a \mu_p \leq b_a$ are also valid solutions for $L\mu_p \leq b$. Propose a supervisor respecting $L_a \mu_p \leq b_a$. Check the transitions involved in the supervisor. Suggest a supervisor respecting $L\mu_p \leq b$ and that t_3 is unobservable.

c) Discuss what changes in the solution of (b) if the columns of D are permuted (e.g. column 2 permutes with column 3) while keeping all the other values.

PS: Do not forget to identify all sheets of paper.

Good Luck,
José Gaspar