Industrial Processes Automation

MSc in Electrical and Computer Engineering
Scientific Area of Systems, Decision, and Control

Winter Semester 2014/2015

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1st Training Laboratory Work [1]

Latch Circuit

The main objective of the 1st training laboratory is to allow the participants to get familiar with the Programmable Logic Controllers (PLCs) Schneider Premium P57 available in the laboratory. In particular are relevant: a) Using the software development system, b) Setting the PLC initial configuration, c) Using the user manuals from Schneider, d) Uploading / downloading programs to/from the PLC, e) Editing and debugging solutions, f) Interfacing with external devices.

Please print and bring this guide to the laboratory. Despite not being graded, it is important to fill and deliver it in the end of the class so that it provides some feedback on the acquaintance obtained in the lab with the hardware.

In this training work are implemented sequential logic circuits using the PLCs available in the laboratory. More in detail, one latch is implemented based in two alternative (combinatorial) logic functions.

Q1. Draw a Ladder diagram implementing the logic circuit described by

X= A OR (NOT(B) AND X)

where **A** and **B** are input signals and **X** is an output.

Q2. Identify the inputs and outputs that will be used in the PLC. In other words, choose two hardware inputs and one output to implement **A**, **B** and **X**. Note that the input and output hardware names depend on the hardware modules mounted in each of the PLCs.

[1] *This training problem has no direct contribution to the final grade.*

Inputs	Hardware identifier / name
A	
B	
Output	
X	

Q3. Download the program to the PLC and execute the program in the PLC. Test your program by setting input values and watching the output. Note: the programming user interface allows forcing (setting) input values; the real input voltages are ignored when the input bits are set to forced.

Q4. Draw a Ladder diagram implementing an alternative latch circuit

X= (A OR X) AND NOT(B)

Test your program using the same hardware inputs and output chosen in the previous question.

Q5. Search in the user manuals how to rename the hardware inputs to the strings ‘in_A’, and ‘in_B’, and rename the hardware output as ‘out_X’. What happens if you try to modify the program while it is under execution?

Q6. Show that the two latch implementations are similar but not exactly equivalent. Suggestions: (i) consider drawing the time responses **X** obtained by varying the inputs **A** and **B**, or (ii) simply writing truth tables having the inputs **A** and **B**, the previous state of the output **X(t-1)**, and the output **X(t)**.